Integration Methods for High-Density Integrated Electric Drives

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Project ID # elt245

Overview

Timeline

- Start Date: *April 2019*
- End Date: *March 2024*
- Percent Complete: 20%

Barriers & Technical Targets

- SiC fabrication facilities and process for heterogeneous integration into power module
- Challenges in high density module fabrication to meet DOE ELT 2025 high voltage power electronics targets:
  - Power density : 100 kW / L
  - Cost : $ 2.7 / kW
  - Peak efficiency : >97 %

Budget

- Total project funding: *$1.5 million*
- Funding for FY20: *$300,000*

Partners

- Virginia Tech
- Oak Ridge National Laboratory

Any proposed future work is subject to change based on funding levels.

Relevance

Overall Objective

To research, develop, and test a heterogeneously integrated power module platform that will insert into a traction inverter system for power electronics modules capable of the following :

Power Electronics Requirements	
Parameter	**Measure**
Cost ($/kW)	≤2.7
Power Density (kW/L)	≥100
System Peak Power Rating (kW)	100

FY 20 Objectives

Advanced SiC module packaging architecture trade-off study and integrated circuit design

- Model-based module architecture study and comparison
- Stacked SiC module and flip-chip module FEA analysis, process preparation, dummy module fabrication
- Selection of decoupling capacitors for integration
- Process/material system preparation and validation
- Integration method study and integrated module design
- High-temperature integrated circuit design in preparation for heterogeneous integration

Any proposed future work is subject to change based on funding levels.

Milestones

FY 20 Milestones

Milestone	Status
Literature review of advanced power module packaging and integration	Complete
Trade-off study to understand module design and its impact to the motor drive system design	Complete
Gate drive, protection, power supply schematic design	Complete
Gate drive, protection, power supply circuit physical design	Complete
Critical IC Design Review	Complete

FY 21 Milestones

Module 3D modeling and parasitic extraction
Process and material system is validated
Module circuit simulation
Go/No Go Decision Dummy module fabrication

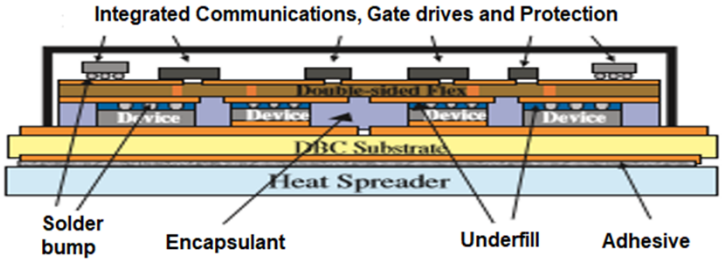
Approach / Strategy

Goal:

The overall project goal is to research and develop a heterogeneously integrated power module platform. The research work involves both integrated circuit design and power electronic module packaging tasks.

Integration Solutions into the Power Module:

- Integrating gate driver and protection circuitry on-chip
- Current and temperature sensors
- Passive filtering
- Cooling solutions: Novel highly conductive materials - TPG



Possible Integration Solution into the Module (Flip chip on flex - FCOF technique)

Heterogeneous Integration Motivation:

- Lower circuit parasitics (lower gate and power loop inductance) for increased efficiency
- Lower footprint
- Higher power density
- Higher system reliability

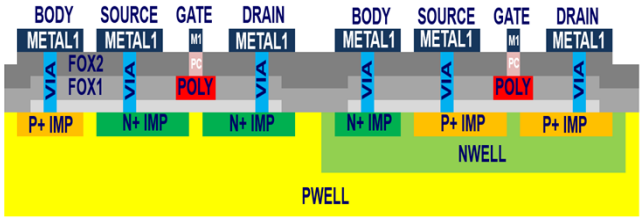
Figure reference : X. Liu and G. Q. Lu, "D/sup 2/BGA chip-scale IGBT package," APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181), Anaheim, CA, USA, 2001, pp. 1033-1039 vol.2. doi: 10.1109/APEC.2001.912493

Technical Accomplishments – FY20

Design of High Temperature Integrated Circuits for Heterogeneous Integration

Process Overview

- University of Arkansas collaborating with Fraunhofer IISB , Germany
- 1 µm SiC CMOS process capable of operating up to at least 300°C
- 50 nm oxide thickness, single metal layer
- Supported devices: NMOS (in P-Well), PMOS (in N-Well), LDMOS, PN Junction diodes, N & P type resistors, Poly Resistors, Capacitors
- Process still developing, characterization underway



Fraunhofer SiC CMOS Cross Section

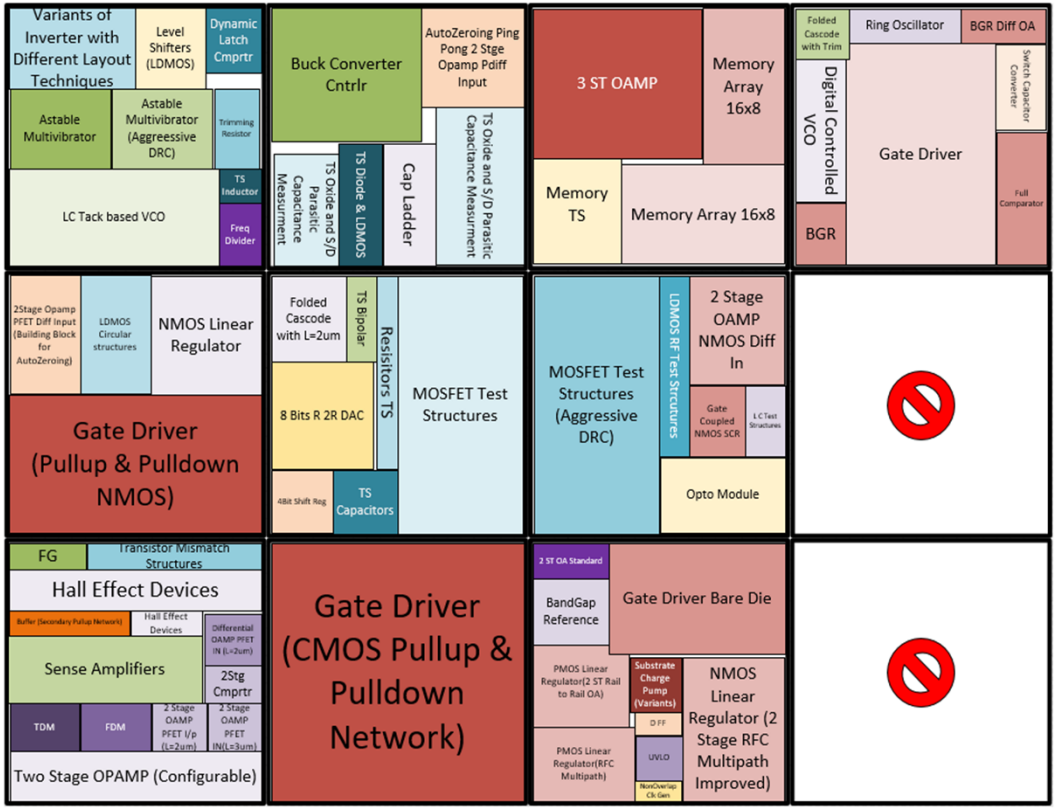
Wafer	1	2	3	4	5	6	7	8	9	10	11	12
Isolation Type	field oxide											
Gate Oxide	50 nm											
PASS0 Doping Reference	X	X					These wafers are held back after implantation and annealing and are expected back later in 2020					
Adjusted NWELL Doping			X	X	X	X						
Polycided (TiSi) Local Interconnection	X		X		X							
P-doped Polysilicon	X	X	X	X								
1 Layer Al and 1 Layer PolySi		X		X	X	X						
1 Layer Pt and 1 Layer PolySi	X		X									
Passivation	X	X	X	X								

Technical Accomplishments – FY20

Fabrication of Silicon Carbide Integrated Circuits

Integrated circuits bill of material:

- Model Parameter Extraction Structure
  - MOSFETs
  - Resistors
  - Capacitors
  - Diodes
  - NPN and PNP BJTs
- Operational Amplifiers
- Comparators
- Power Management Circuits
  - Bandgap Voltage Reference
  - Linear Regulator
- Gate Driver
  - Controllable drive strength
  - Includes protection circuits
- Digital to analog converters
- Ring oscillators, VCO
- Flip-flop, Registers, SRAM
- Hall effect devices

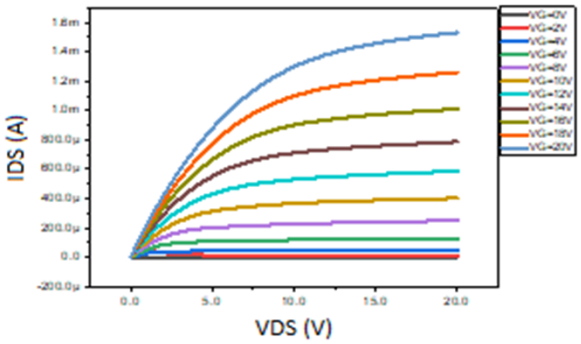


High Temperature Low voltage SiC Chip Map

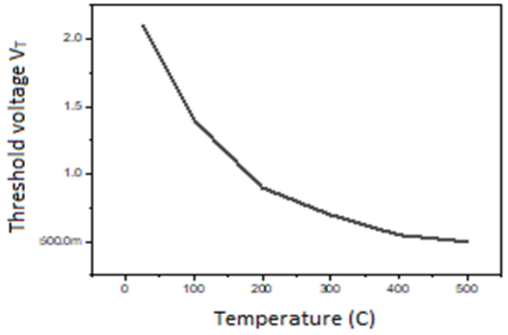
Technical Accomplishments – FY20

Characterization of SiC Low-voltage Devices over Extreme Temperature

500°C

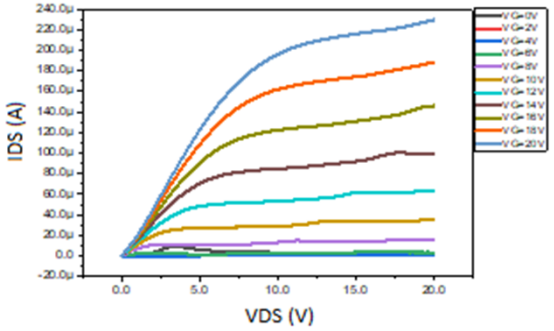


20/2 µm NFET at 500°C



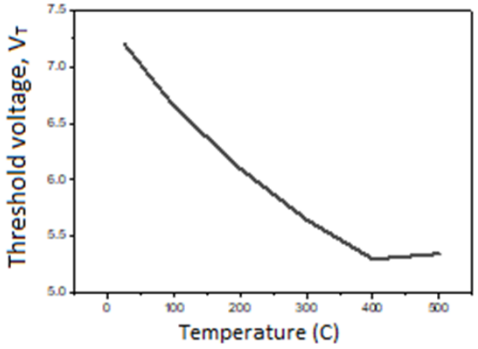
NFET threshold voltage over temperature

500°C



20/2 µm PFET at 500°C

- ✓ Current drive increases with increase in temperature for same Vgs from 100°C to 400°C for both NFET and PFET
- ✓ From 400°C to 500°C current drops, although not significantly
- ○ High P+ ohmic contact resistance results in lower current carrying capability and Schottky type behavior in triode region



PFET threshold voltage over temperature

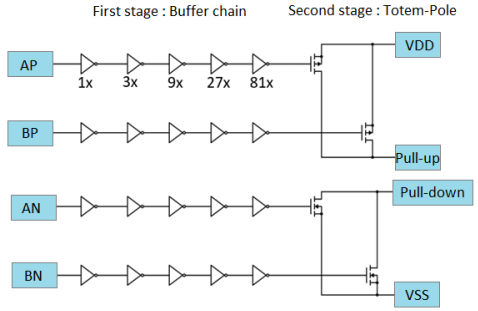
Technical Accomplishments – FY20

High Temperature SiC Gate Driver Chip Heartbeat Evaluation ONLY on Probe Station

- ✓ Several driver topologies designed with different numbers of drive slices
- ✓ Functionality verified for a driver with two CMOS drive slices driven by buffer chains
- ✓ Test in progress for other driver topologies at elevated temperatures

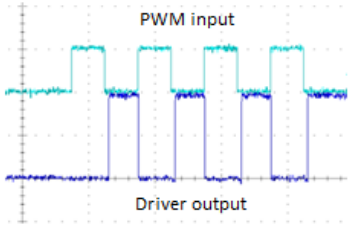
Test condition:

- Room temperature 13 pF probe load
- VDD limited to 10 V to avoid excessive overshoots induced by probe parasitics.

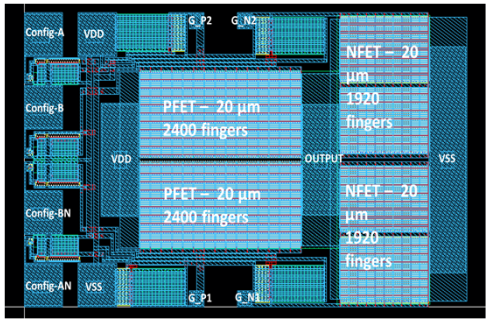


Simplified Driver Schematic

VDD	Input Frequency	Rise time	Fall time
7 V	1 kHz	40 µs	7 µs
8 V	10 kHz	10 µs	2.5 µs
10 V	100 kHz	1.5 µs	700 ns



Driver Test Results



Layout dimension 3.70 mm x 2.13 mm

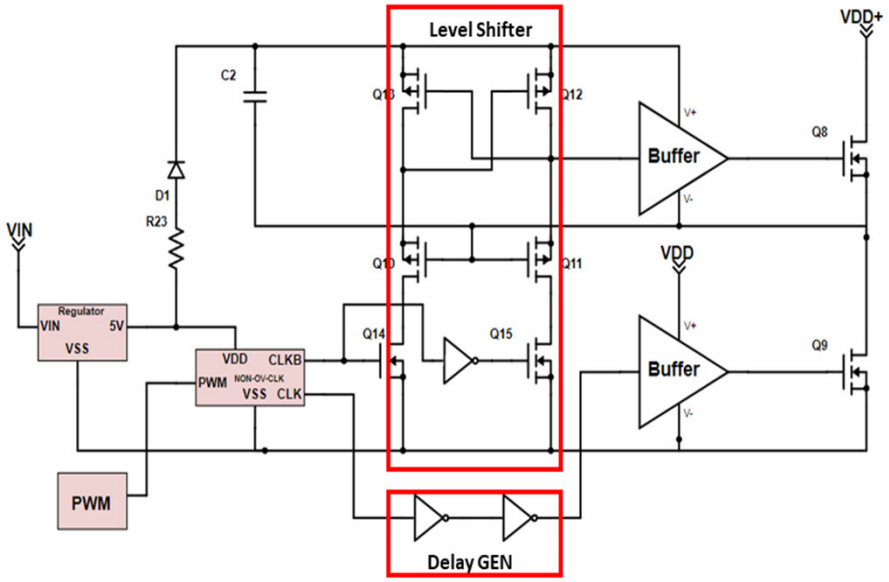
Technical Accomplishments – FY20

Integrated Chip Gate Driver in SOI Process as Risk Mitigation Plan

Gate driver in XFAB XT018 – 0.18 µm HV SOI CMOS process taped-out in January 2020 as part of risk mitigation plan

Driver Characteristics:

- 2.5 A sink / source capability with output swing of 15 V to -4 V
- Includes local bootstrap technology as gate voltage cannot exceed 5.5 V
- Protection circuity includes overcurrent protection, under-voltage lockout (UVLO) and V_{DS} sensing circuits.



SOI Gate Driver

Technical Accomplishments – FY20

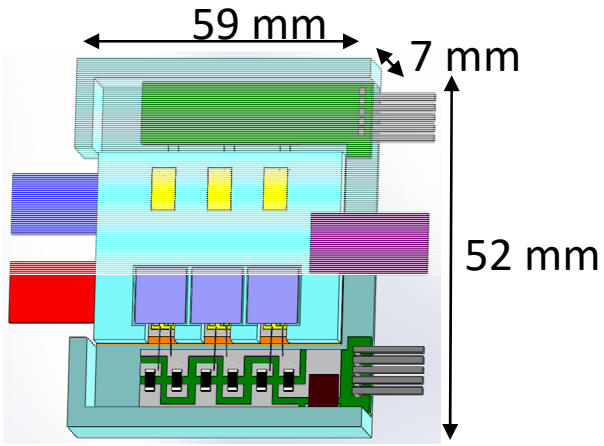
Double-sided Stacked Power Module Design in Preparation

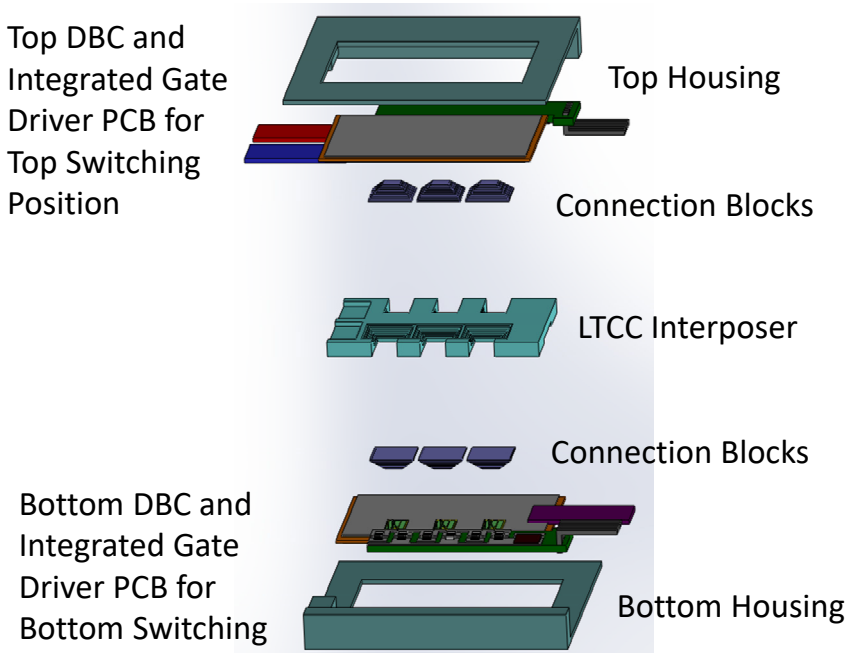
Pros:

- Short fabrication time

Cons:

- More complicated housing design
- Need gate electrode wire bonding



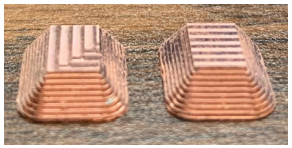


Double -sided stacked power module

Technical Accomplishments – FY20

Completion of Thermal Simulation of the Power Module

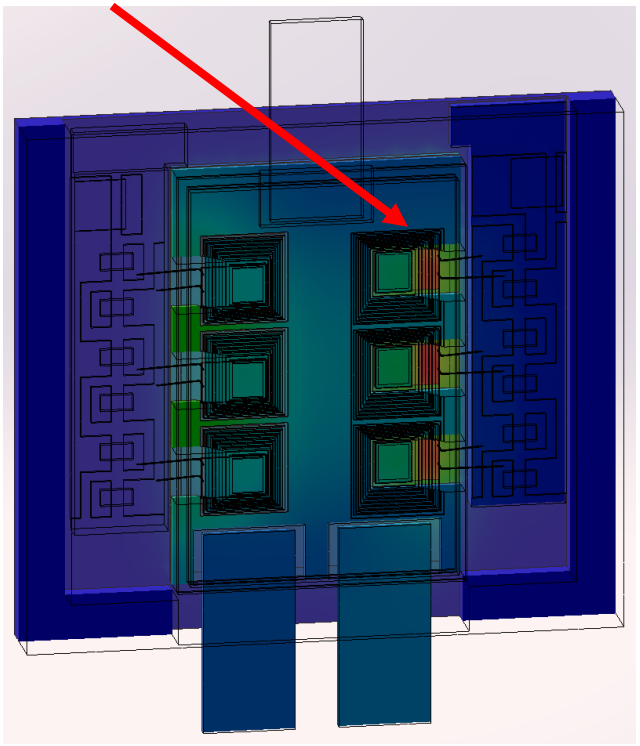
Thermal Simulation Using Pyramidal Blocks



Specification	Value
Voltage	1200 V
Current	135 A @ T_j=175°C
Stray Inductance	6.6 nH

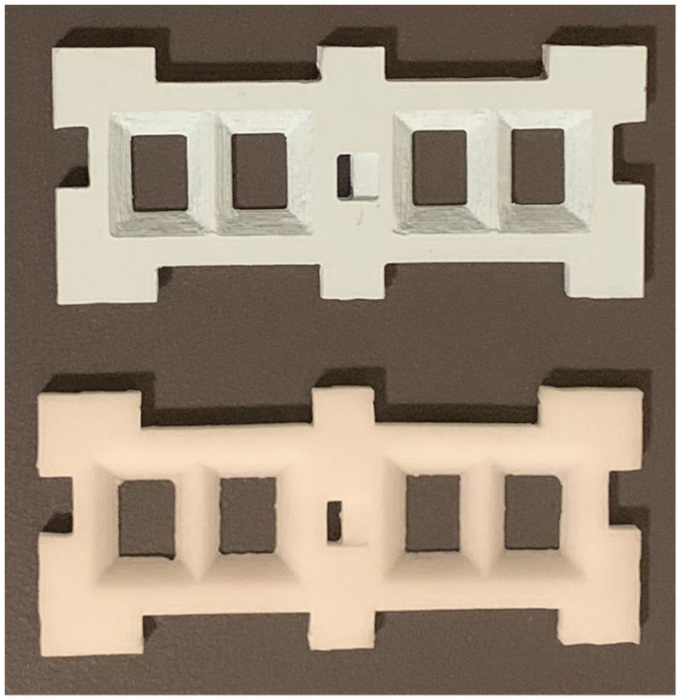
Thermal Load	Value
Power (Per Item) (W)	52
Internal Resistance (mΩ)	26
Convection Coefficient (W/m²K)	10000
Ambient Temperature (°C)	65

Maximum Temperature: 175°C



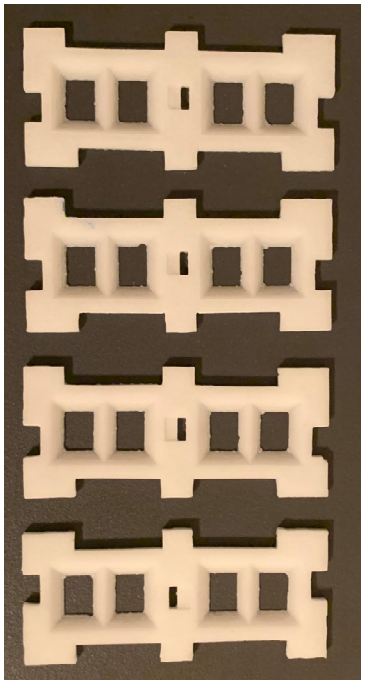
Technical Accomplishments – FY20

Fabrication of Ceramic Interposer using Ceramic 3D Printer and LTCC



3-D Print

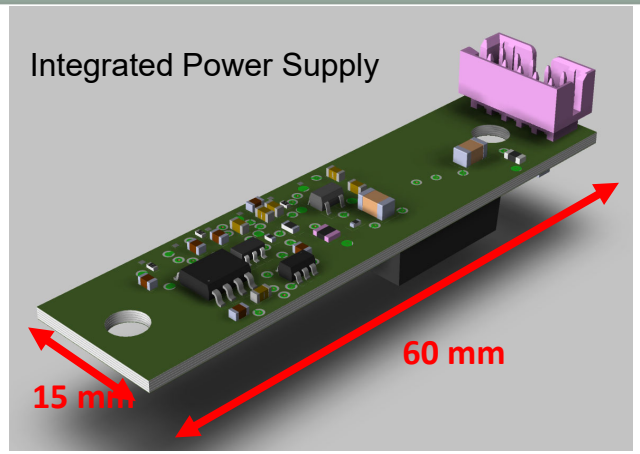
LTCC Procedure

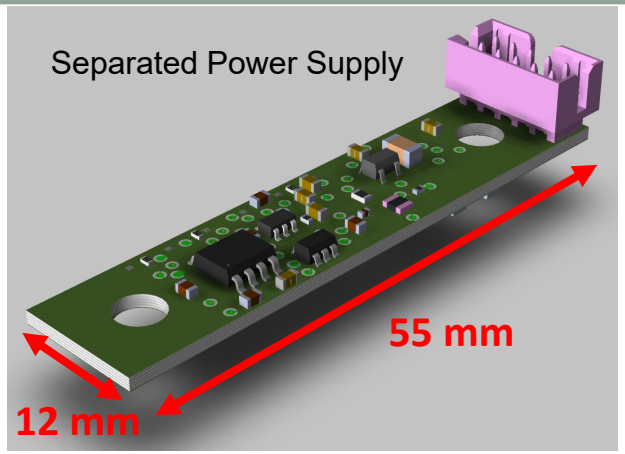


Interposer Fabrication

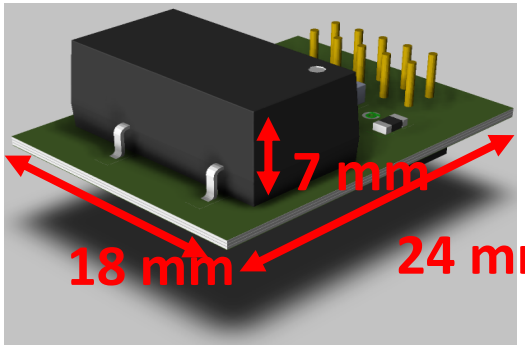
Technical Accomplishments – FY20

Two Gate Driver Boards Designed for the Power Module Prior to Gate Driver IC Integration Into Module





Six-Layer Gate Driver Board



Technical Accomplishments – FY20

Study of Comparative Performance of Different Current Sensing Techniques

	Cost	Bandwidth	DC capability	Sensitivity	Saturation	Linearity	Operating temperature	Footprint
Shunt resistors	low	DC~10 MHz	yes	5 mV/A	no	very good	-55~125 °C	8×6×2.5 mm
Rogowsky coil	low	0.1~100 MHz	no	10 mV/(A/μs)	no	very good	-20~100 °C	O.D.<20 mm, Height<4 mm
Hall sensors	high	< 1 MHz	yes	10 Gauss	yes	poor	-40~125 °C	6×5×1.7 mm
GMR sensors	medium	DC~5 MHz	yes	10-2 Gauss	yes	fair	-40~150 °C	1.2 ×0.7mm
Current Transformer	medium	0.1 Hz~100 MHz	no	1 V/A	yes	fair	-50~150 °C	N.A.
GMI sensors	medium	DC~ 30 GHz	yes	10-6 Gauss	no	fair	-40~150 °C	4×3mm

✓ One from the summarized techniques will be selected for integration based on the requirement from the power module package design which is to be finalized later in this project.

Technical Accomplishments – FY20

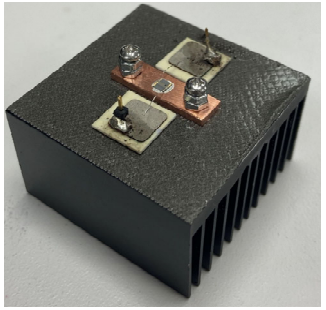
Experimental Verification of Integrated Cooling Solution with TPG

Metal Encapsulated Thermal Pyrolytic Graphite (TPG) overview :

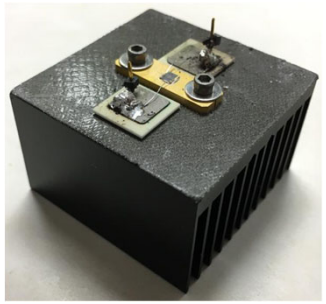
- Anisotropic material
- High in-plane (X-Y) thermal conductivity(~1700 W/mK)
- Low through plane(Y-Z and X-Z) plane thermal conductivity

Experimental setup :

- Heat dissipated (resistor): 10 W
- Convection Co-efficient: For forced air cooling

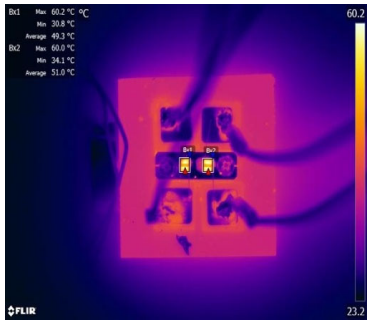


Copper substrate



Metal encapsulated TPG substrate

FEA and experimental results to verify better thermal performance of TPG over copper:



Experimental result shows decrement of 10℃, where FEA simulation showed 9℃ in case of TPG substrate

Responses to Previous Year Reviewer's Comments

- This project is a new start

Collaboration and Coordination with other Institutions

Virginia Tech

- Design of double-side cooled power module with DBC/IMS
- Processing and characterization of sintered-metal interconnect
- Packaging of high-temperature gate driver IC from UA

Oak Ridge National Laboratory

- High Performance Liquid Cooled Heat Sink Design
- Insulated Metal Substrate Development for Single and Double Sided Packaging
- System Integration and Evaluation

Remaining Challenges and Barriers

- To get a reliable SiC CMOS process with reduced P+ contact resistance and increased current carrying capability to design efficient gate driver
- Metalizing the gate / source pads of SiC dies by University of Arkansas to make the layout design of a double-sided module much easier and more optimized
- The power module fabrication is challenging and a few LTCC and 3D printing steps will be taken (as was done for the interposer fabrication) to reach to the ideal housing design

Any proposed future work is subject to change based on funding levels.

Proposed Second Year Work – FY 21

High Temperature Gate Driver Design:

- To fully characterize the Fraunhofer SiC CMOS process and test the fabricated gate driver variants on that process at elevated temperature.
- To analyze those results as learning steps for next SiC CMOS fabrication run

High Power Density Power Module Design:

- Gate driver PCBs assembly and testing
- Metallization of the bare dies
- Fabrication of the power module housing
- Power module assembly and testing

Integrated Solutions for Power Module:

- Design of an integrated power electronics module (IPEM) with all the possible integration solutions studied according to the project requirements in terms of cost, power density (≥100 kW/L) and system peak power rating (100 kW)

Any proposed future work is subject to change based on funding levels.

Summary

Relevance:
To research, develop, and test a heterogeneously integrated power module platform

Approach:
- To design a high power density power module
- Integration of gate driver, current sensors, passive filtering and cooling technique

Collaborations and Coordination with other institutions:
- *Virginia Tech* – Designing double sided cooled power module and packaging gate driver
- *Oak Ridge National Laboratory* – Designing high performance heat sink and developing IMS, system integration and evaluation

Technical Accomplishments:
- Characterization run on high temperature SiC CMOS process
- Study of double-sided power module arrangements to learn the overall system compatibility of a power module design
- Study of different integration components: current sensors, temperature sensors, gate driver integration techniques and novel cooling solutions.

Future Plan:
- To determine next high temperature CMOS fabrication run for gate driver circuitry
- To design integrated power module with all the possible integration solutions studied

Any proposed future work is subject to change based on funding levels.

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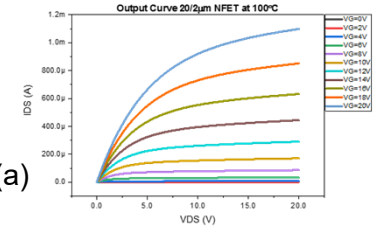
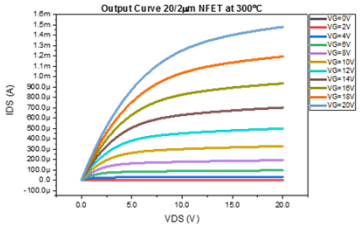
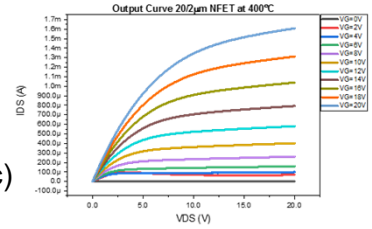
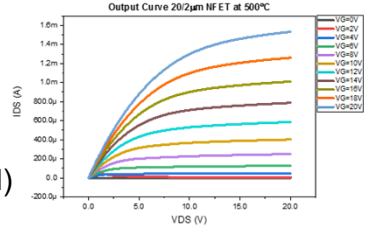
Technical Back – Up Slides

Technical Back-Up Slides

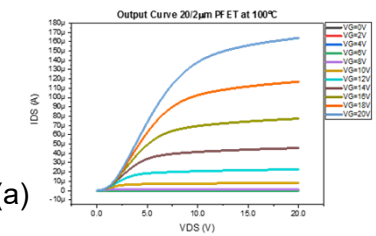
(a) 

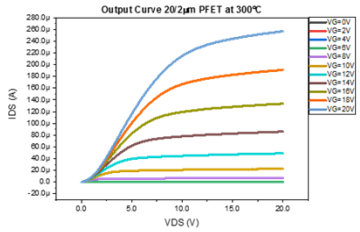
(b) 

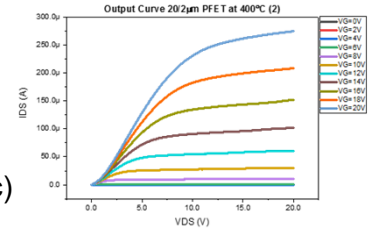
(c) 

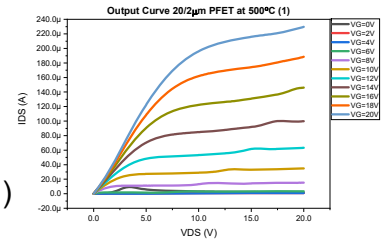
(d) 

I_D-V_{DS} curves of the NFET for the width of 20µm and length of 2µm at (a) 100ºC (b) 300ºC (c) 400ºC (d) 500ºC

(a) 

(b) 

(c) 

(d) 

I_D-V_{DS} curves of the PFET for the width of 20µm and length of 2µm at (a) 100ºC (b) 300ºC (c) 400ºC (d) 500ºC

Technical Back-Up Slides

Temperature Range of Gate Driver Board Components	
SMD Capacitors	-40°C ~ 125°C
SMD Resistors	-55°C ~ 155°C
Multilayer Inductors	-55°C ~ 125°C
General Purpose Digital Isolator	-40°C ~ 125°C
Gate Driver IC (TI Si UCC27531)	-40°C ~ 140°C
Isolated Module DC DC Converter	-40°C ~ 105°C (With Derating)
Receiver	-40°C ~ 125°C

✓ The higher the temperature characteristics of a component, the bigger the footprint size

Technical Back-Up Slides

Shunt Resistor

- Technology: measurement of ohmic voltage drop

Integration in Power Modules:

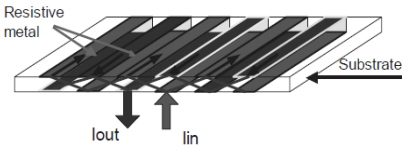
- Thick film metallization processing.
- Interleaving parallel metal strips deposited onto both sides of a thin kapton substrate.
- Metal strips on opposite sides and neighboring strips bear opposite current, resulting in low inductance and wide bandwidth.
- Standard 2 terminal shunt may have significant error from contact resistance and lead resistance, 4 terminal kelvin connection hence is used.

Rogowski Coil

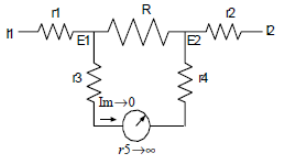
- Technology: voltage induced in air-cored coil wrapped in a toroidal fashion, proportional to rate of change of current, is integrated to get proportional output current

Planar embedded Rogowski coil

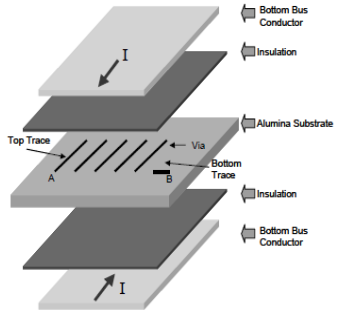
- Embedded coil in between two bus conductors which carry balanced current, no extra shield to avoid external noise needed.
- Parallel conductor traces on both sides of alumina substrate connected by vias.



Integrated planar shunt



4 terminal kelvin connection



Proposed Rogowski coil

Figure reference: Chucheng Xiao, Lingyin Zhao, T. Asada, W. G. Odendaal and J. D. van Wyk, "An overview of integratable current sensor technologies," 38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003., Salt Lake City, UT, USA, 2003, pp. 1251-1258 vol.2.

Technical Back-Up Slides

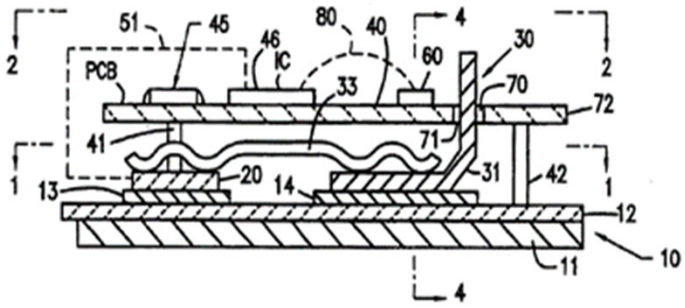
Integration of Hall Effect Sensors in Power Modules :

- L shaped current carrying bar (30) carries drain current.
- Hall effect sensor (60) produces output voltage proportional to magnetic field and thus, drain current, to be coupled back to IC 46, for desired MOSFET(20) control.

GMR Sensors (current and temperature detector):

- Technology: Constructed from a material which changes its resistance when exposed to the magnetic field. Four resistors arranged in wheat stone bridge form.

Integration in Power Modules



Cross section of power module with Hall sensors integrated

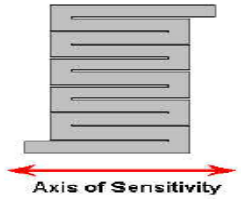
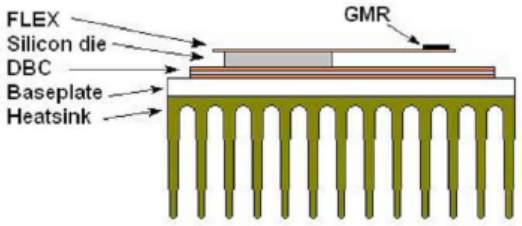
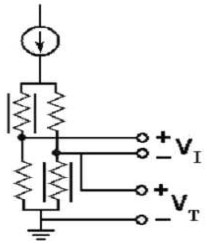


Photo-etched, planar, GMR serpentine



GMR detector with FLEX interconnect



GMR as field and temperature sensor simultaneously

Figure reference :W. Kim, S. Luo, G. Lu and K. D. T. Ngo, "Integrated current sensor using giant magneto resistive (GMR) field detector for planar power module," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2013, pp. 2498-2505.
H. N. Shah et al., "Power electronics modules for inverter applications using flip-chip on flex-circuit technology," Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting., Seattle, WA, USA, 2004, pp. 1526-1533 vol.3.